

Figure 1 – Hardware Architecture

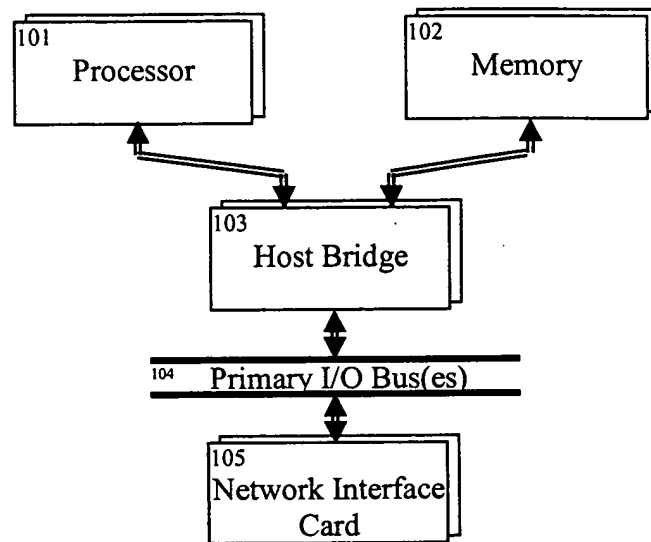


Figure 2 – NIC Hardware Architecture

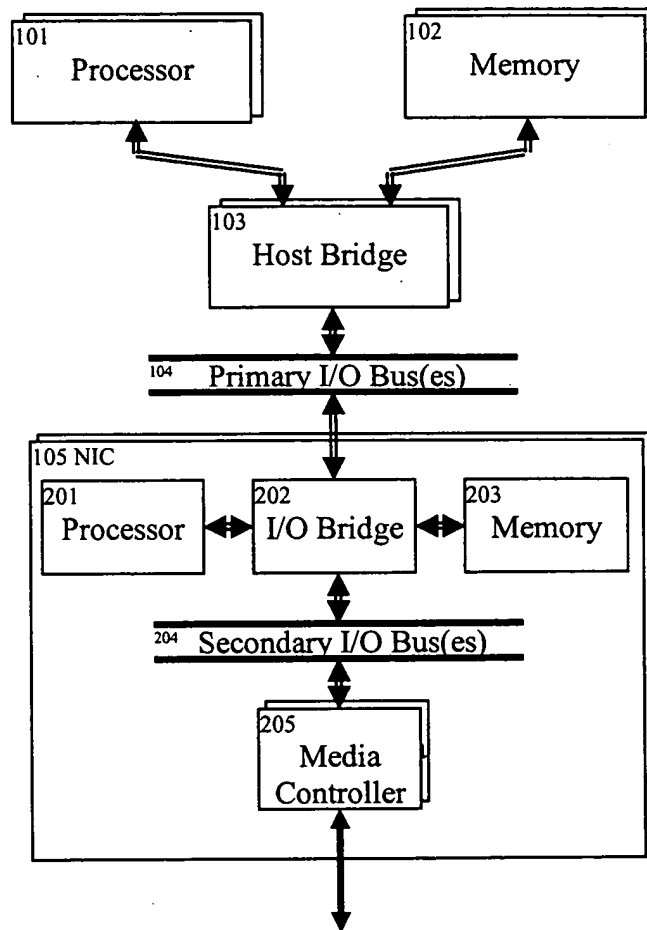


Figure 3 – Vito NIC Hardware Architecture

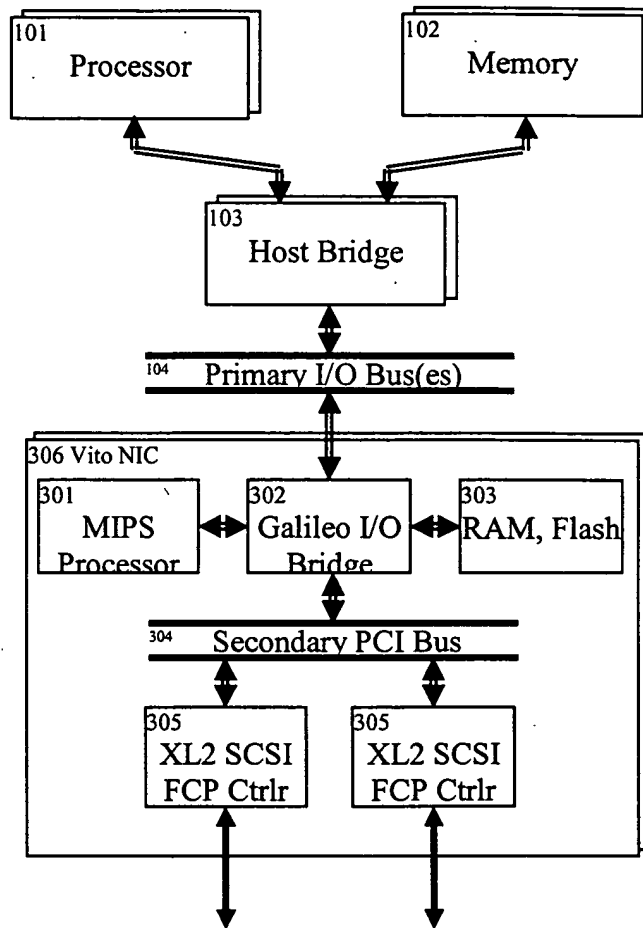


Figure 4 – Vito Software Architecture

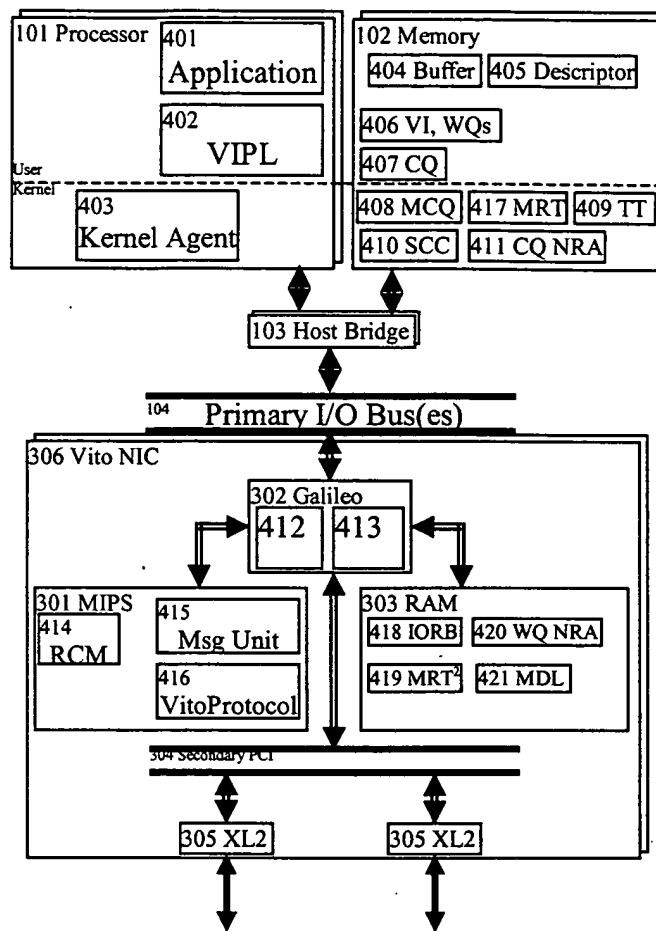


Figure 5 – Memory Registration Message Flows

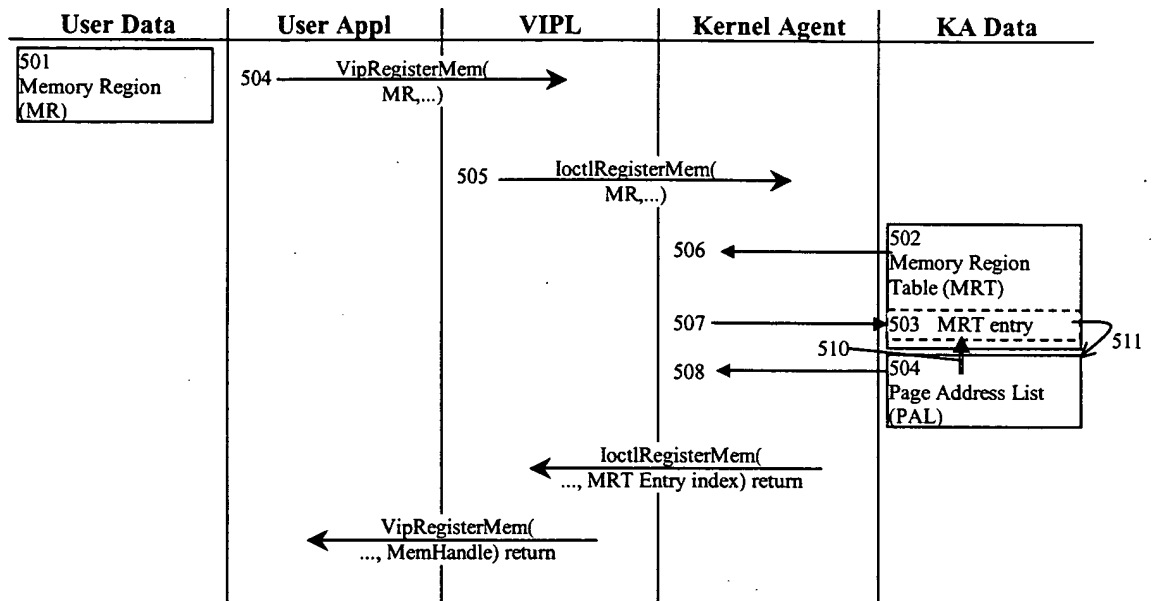


Figure 6 – Descriptor Posting Message Flows

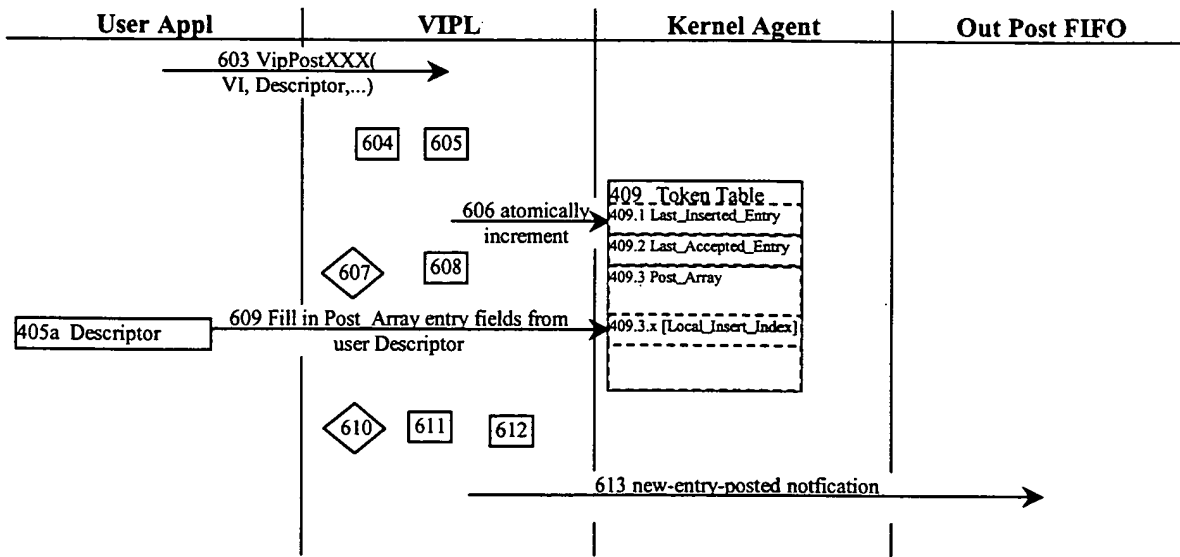


Figure 7 – Msg Unit Descriptor Processing Message Flows

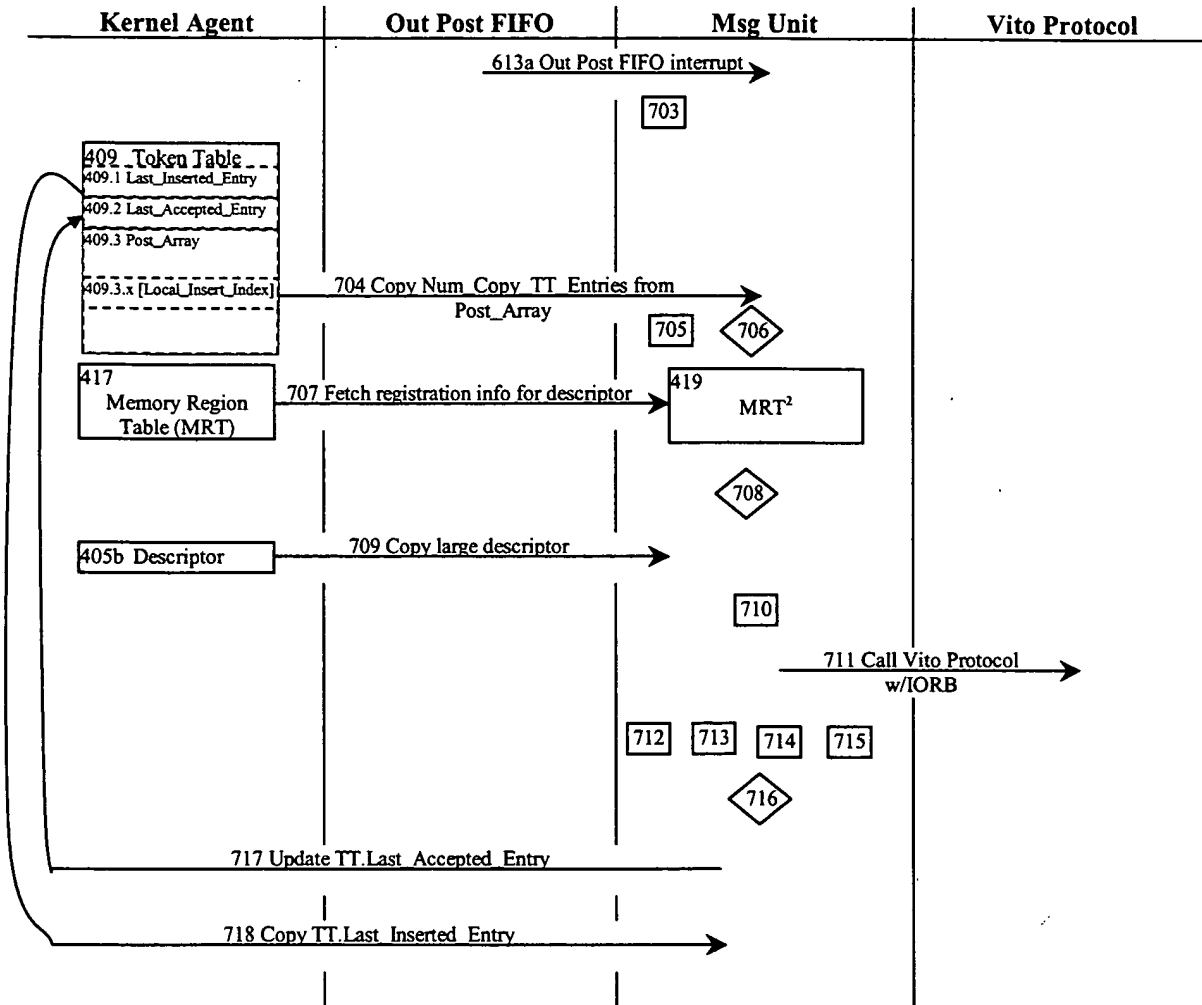


Figure 8 – Send Processing Message Flows

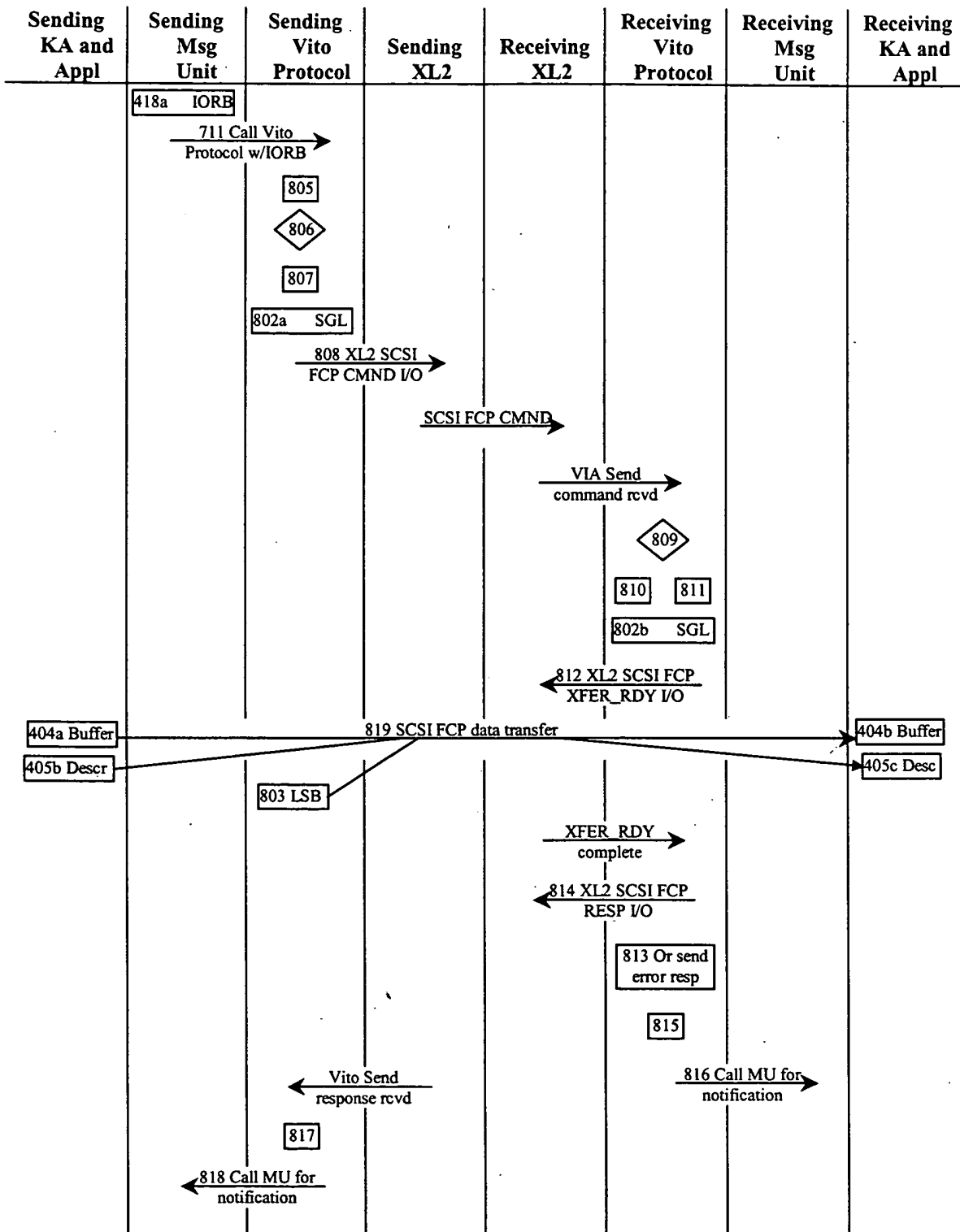




Figure 9 – RDMA-Write Processing Message Flows

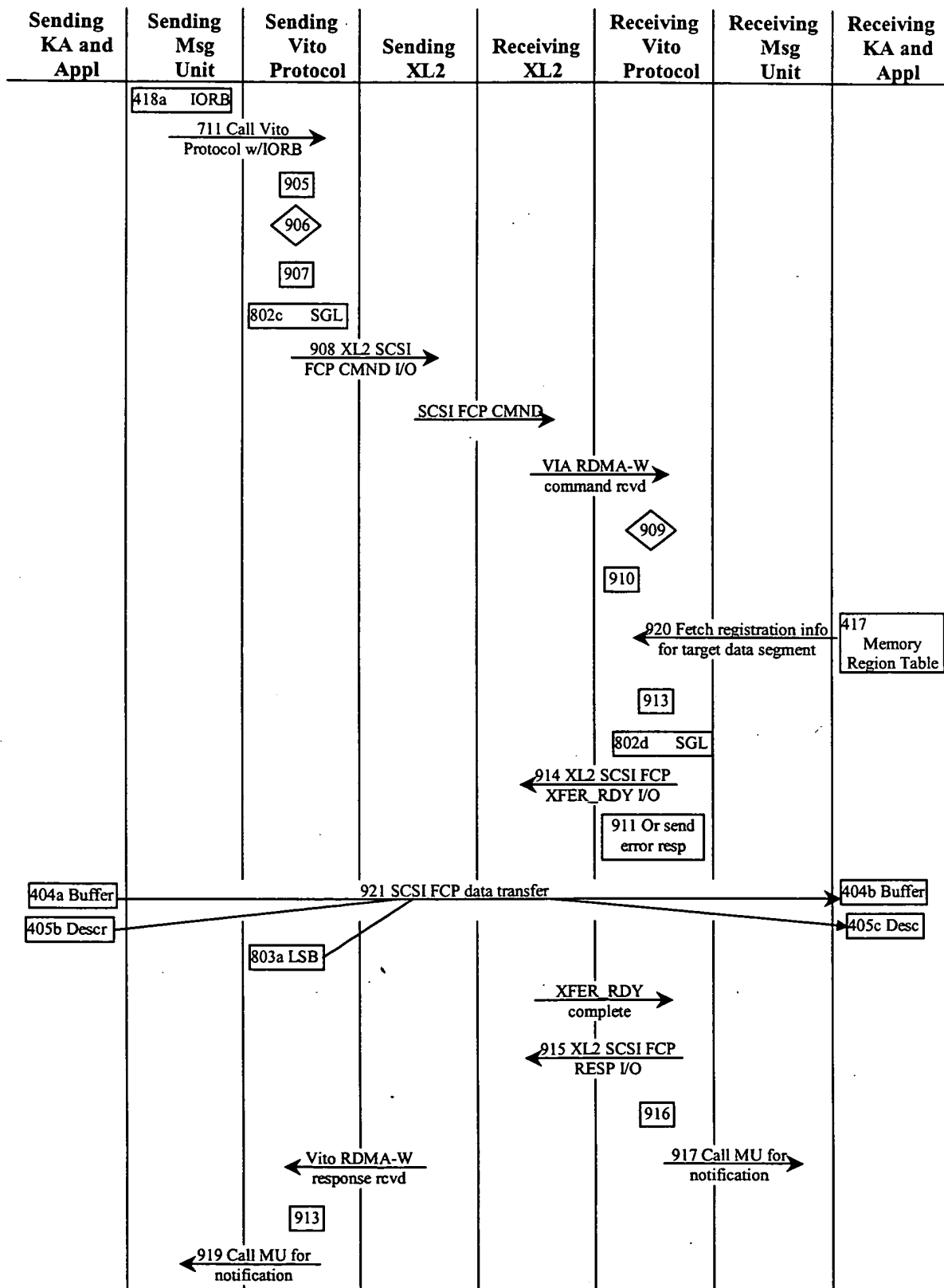


Figure 10 – RDMA-Read Processing Message Flows

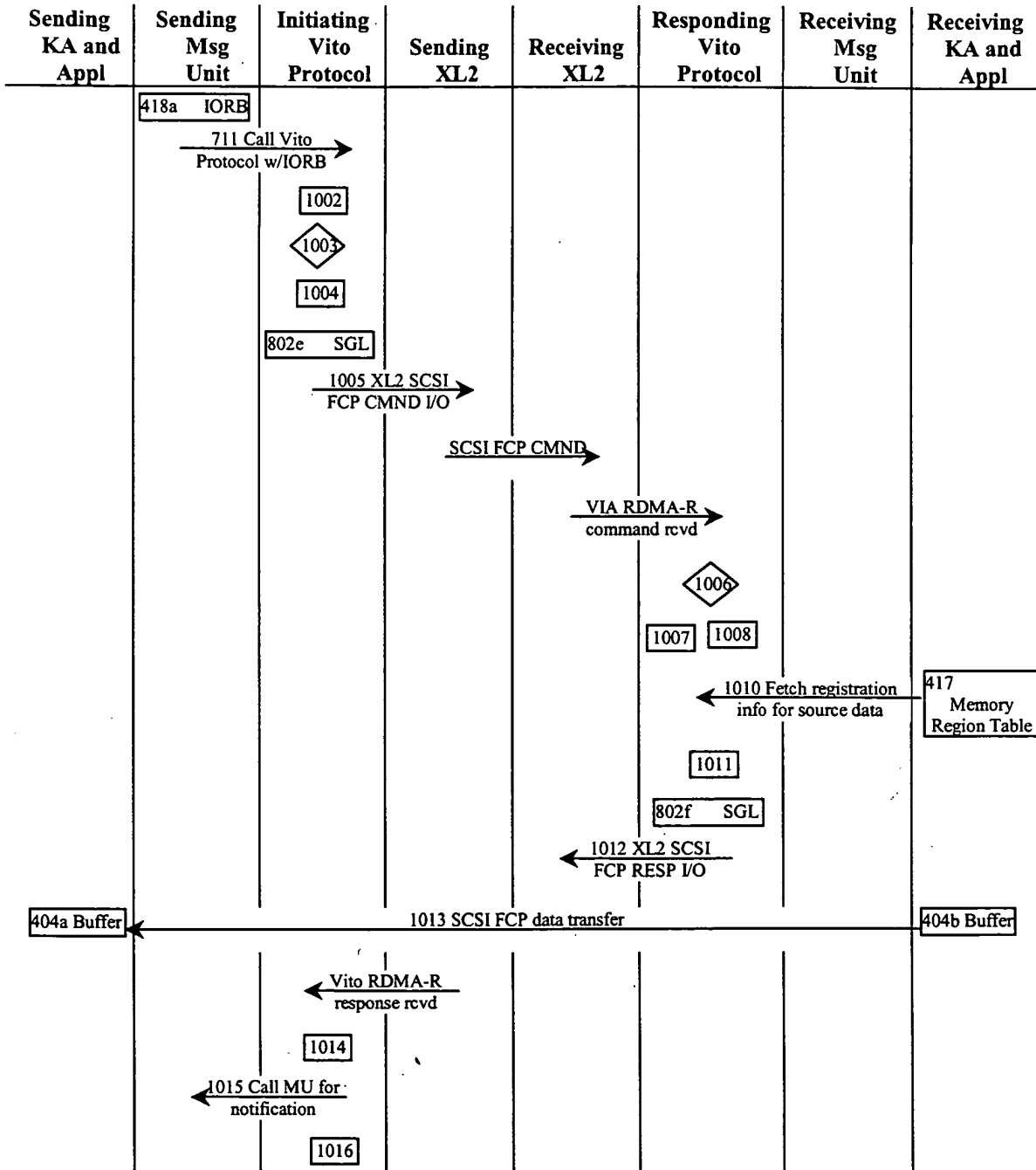


Figure 11 – Work Queue Completion Notification Message Flows

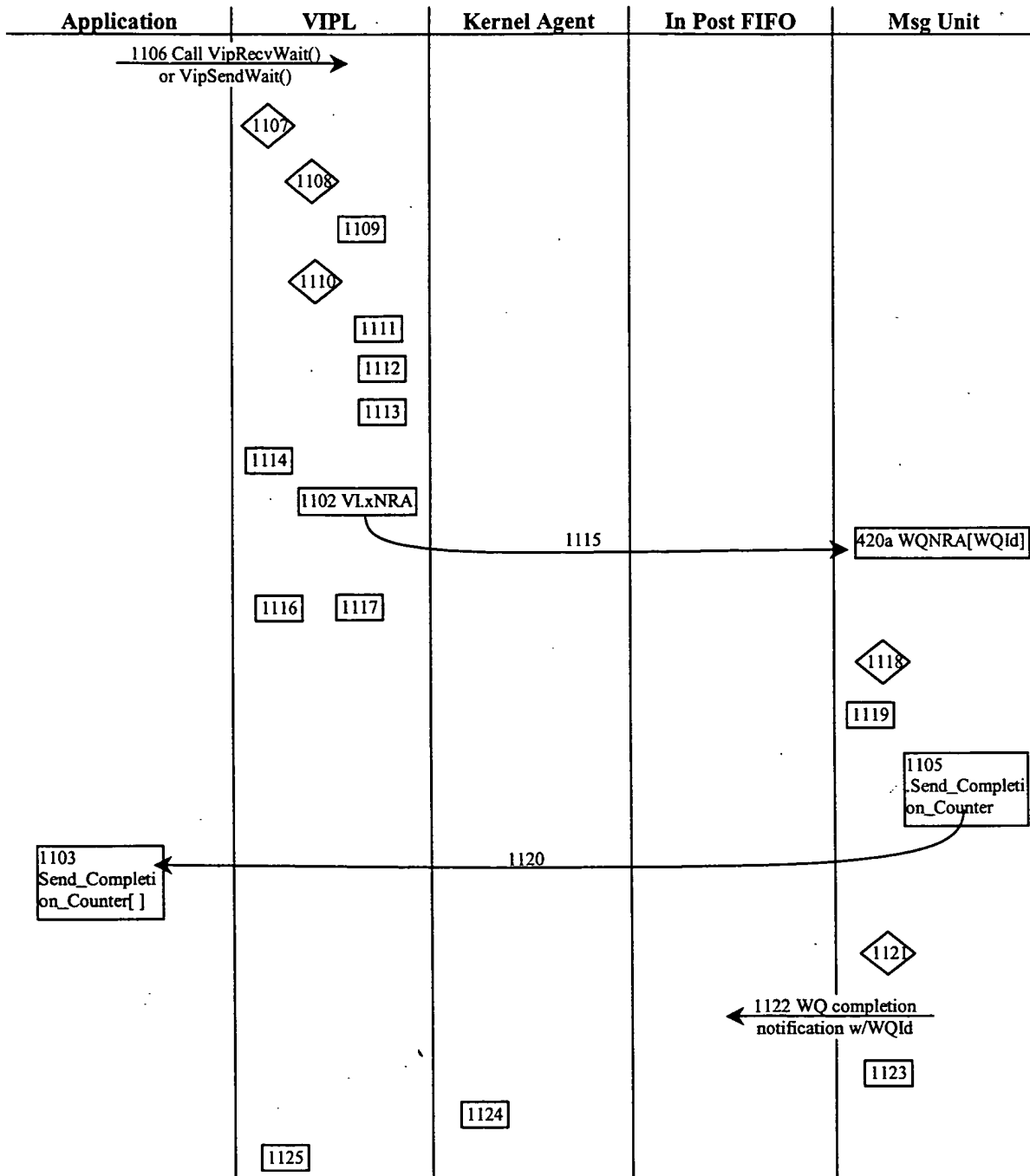
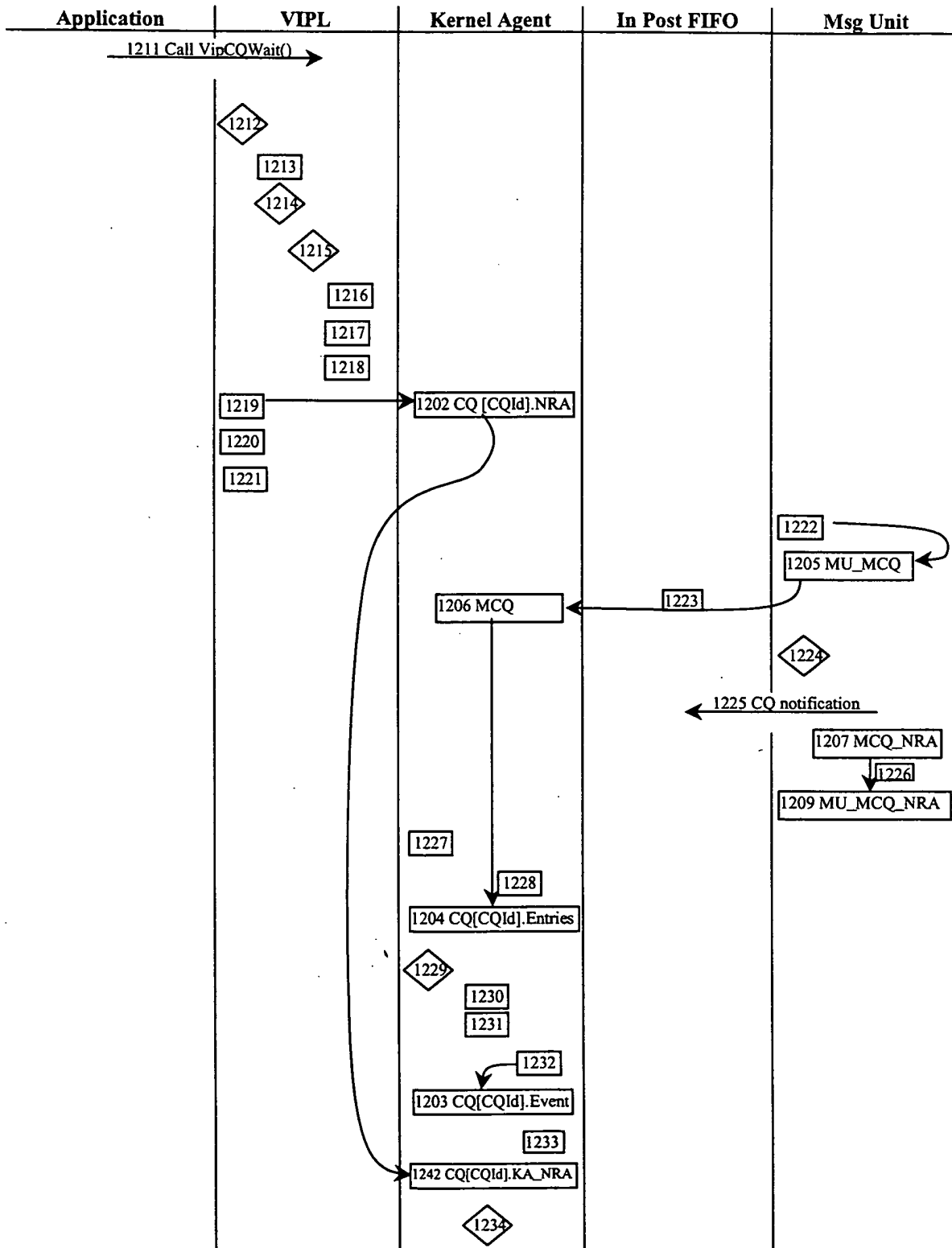


Fig. 12.1

Figure 12 – Completion Queue Completion Notification Message Flows



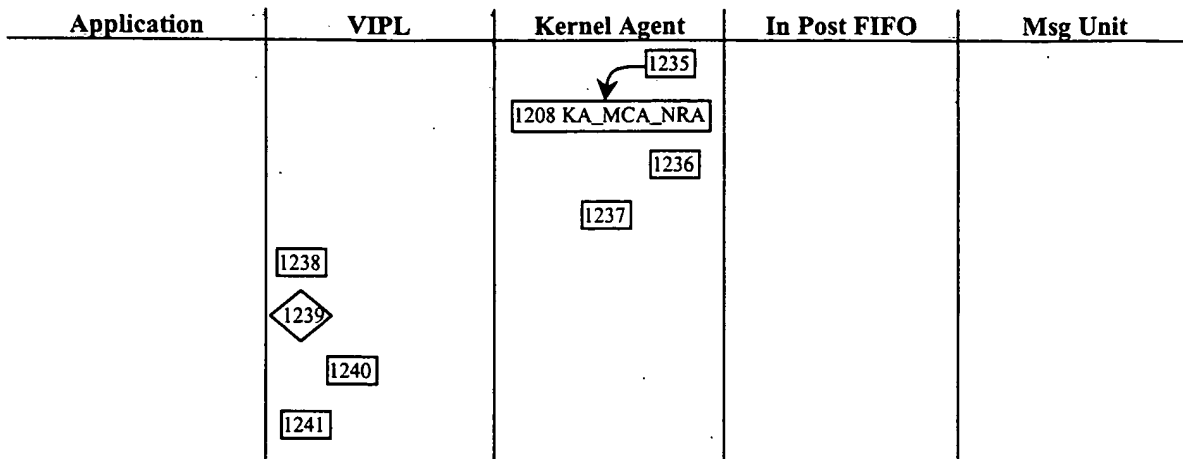


Fig. 12.2

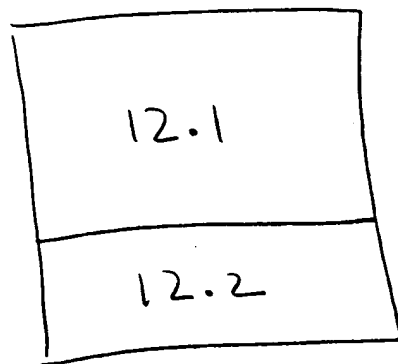
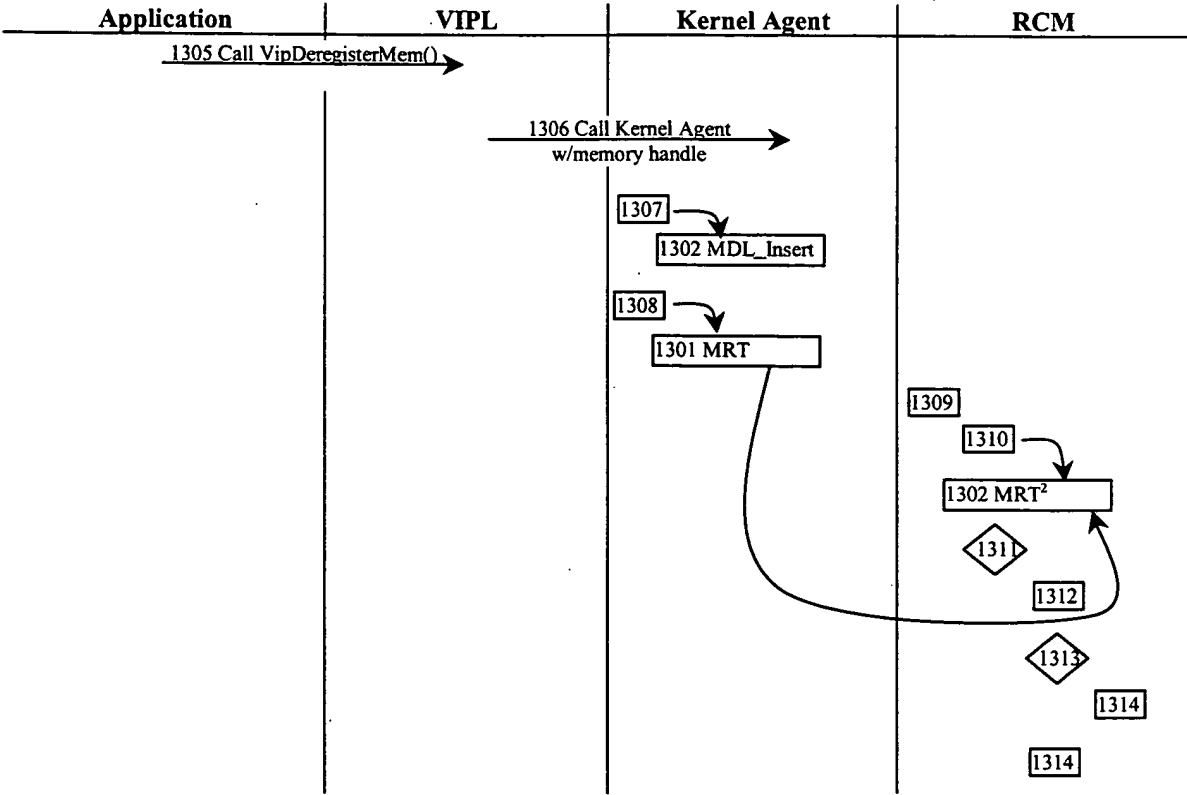


Figure 13 – Memory Deregistration Message Flows



# Figure 14 – Vito-FC FCP\_CMD IU Updates

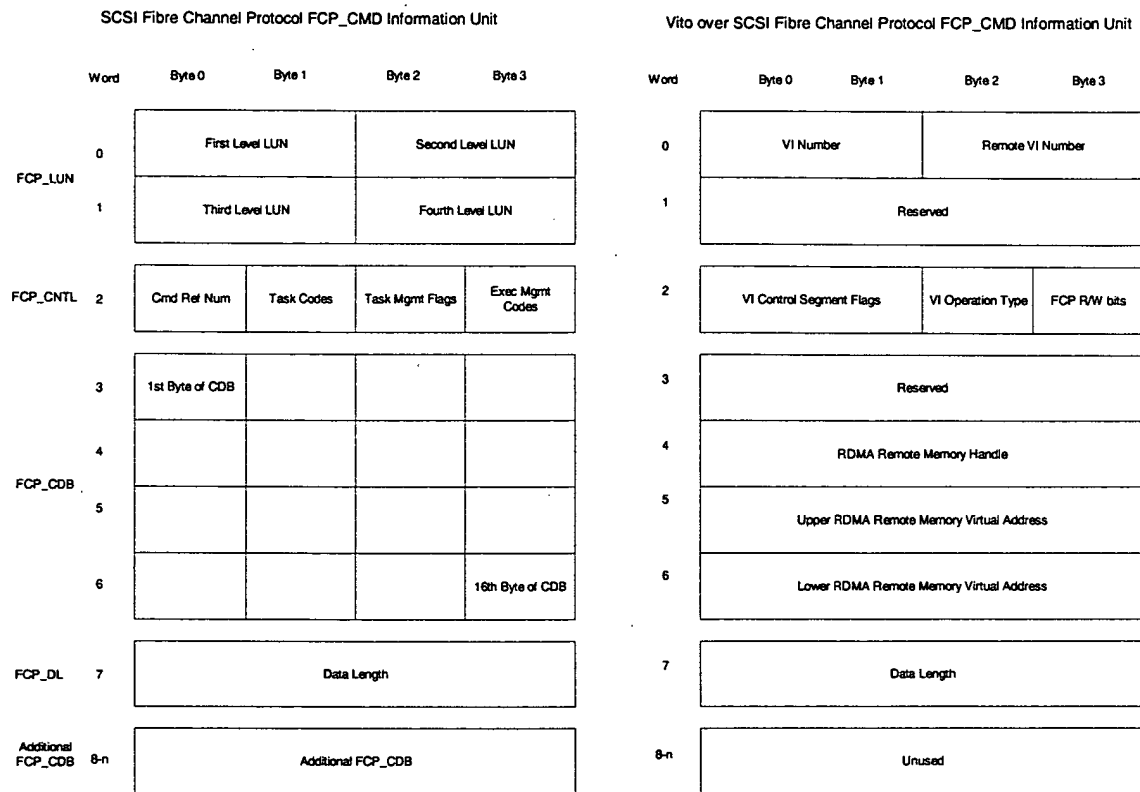


Figure 15 – Vito-FC FCP\_RESP IU Updates

SCSI Fibre Channel Protocol FCP\_RESP  
Information Unit

Word	Byte 0	Byte 1	Byte 2	Byte 3
0				
reserved				
1				
FCP_STATUS	2	reserved	reserved	Validity Flags SCSI Status Byte
FCP_RESID	3			
FCP_SNS_LEN	4	(length of FCP_SNS_INFO in bytes)		
FCP_RSP_LEN	5	(0, 4, or 8 bytes per FCP)		
6	reserved	reserved	reserved	RSP_CODE
FCP_RSP_INFO	7	reserved	reserved	reserved
FCP_SNS_INFO	8-n	(Variable length as defined by the FCP_SNS_LEN)		

Vito over SCSI Fibre Channel Protocol FCP\_RESP  
Information Unit

Word	Byte 0	Byte 1	Byte 2	Byte 3
0				
1				
2	reserved	reserved	Validity Flags	SCSI Status Byte
3				
4	(0=Good FCP_RESP and 8=Bad FCP_RESP)			
5	(0=Good FCP_RESP and 8=Bad FCP_RESP)			
6	reserved	reserved	reserved	RSP_CODE
7	reserved	reserved	reserved	reserved
8-n	VI Status Code			



Fig. 16

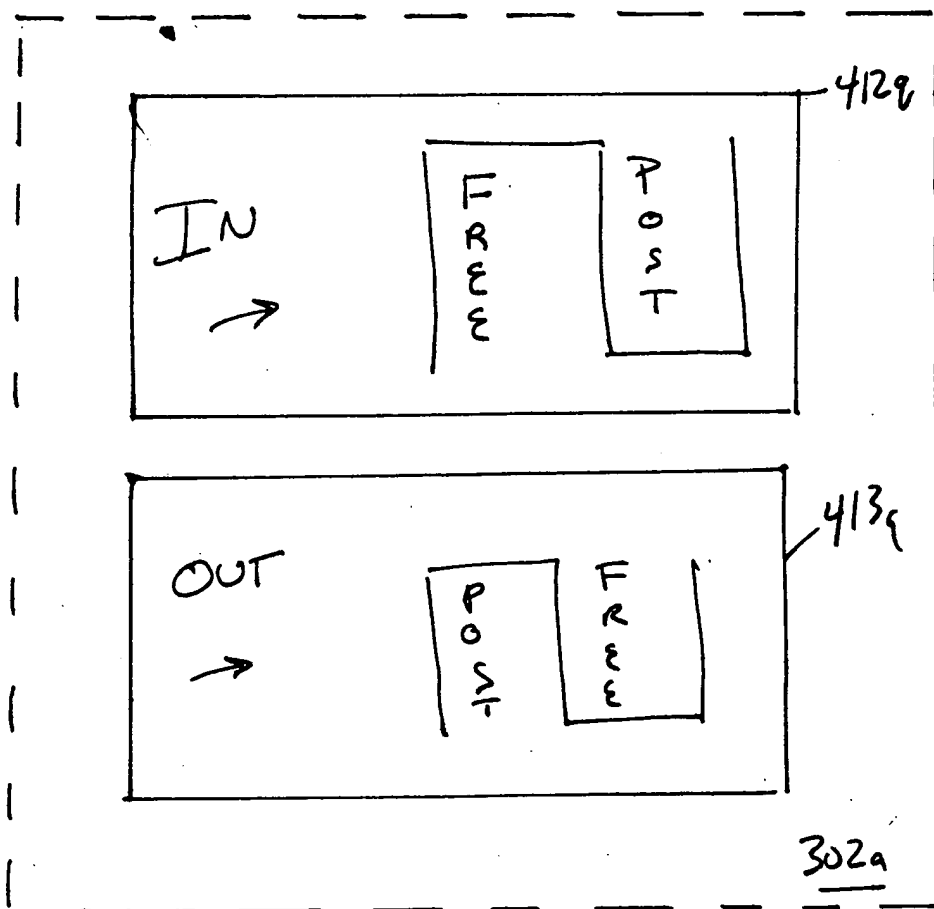
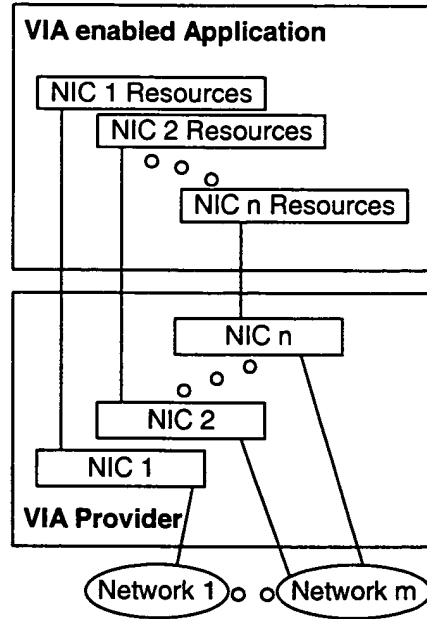


Figure 17

Application perspective:  
Standard VIA Provider



Application perspective:  
PICNIC VIA Provider

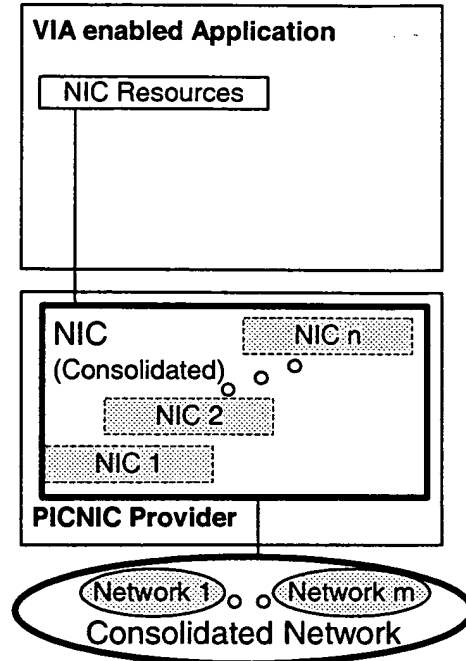


Figure 18 – PICNIC Data Structures

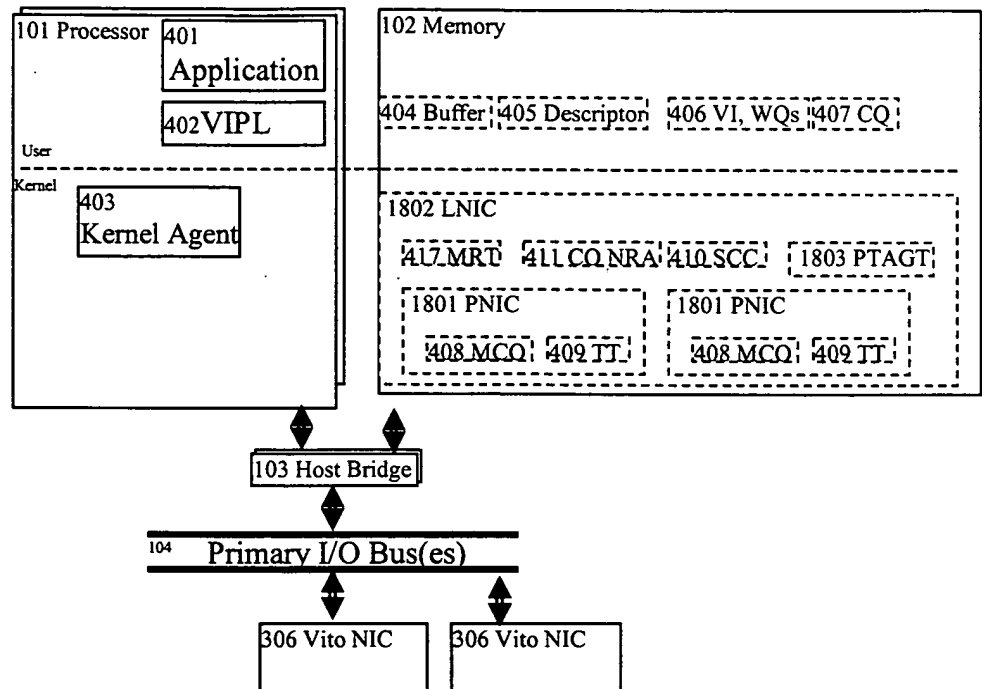


Figure 19 – Possible Link Configurations

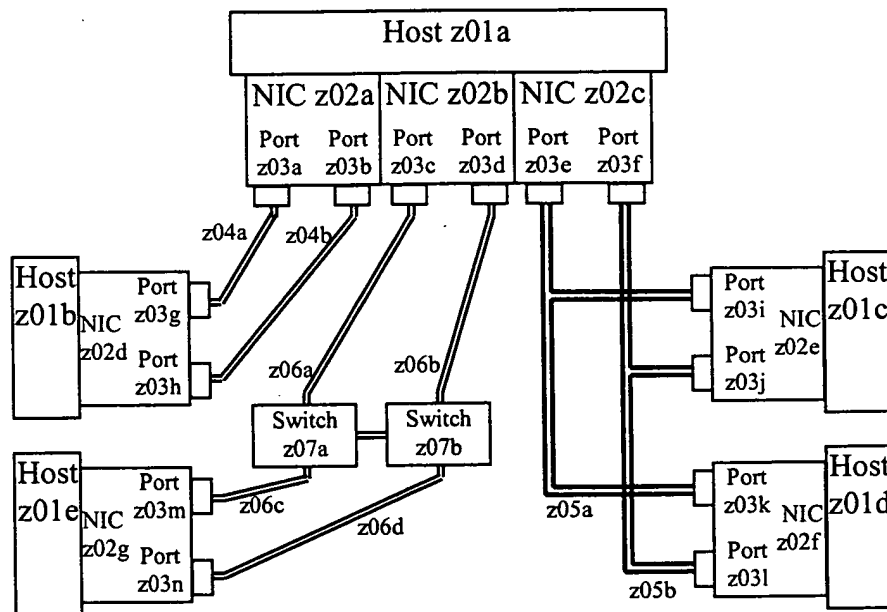


Figure 20 – Example Paths

Host		z01a						z01b		z01c		z01d		z01e	
	Port	z03a	z03b	z03c	z03d	z03e	z03f	z03g	z03h	z03i	z03j	z03k	z03l	z03m	z03n
z01a	z03a	Lb						z04a							
	z03b		Lb						z04b						
	z03c			Lb	z06a; z07a; z07b; z06b									z06a; z07a; z06c	z06a; z07a; z07b; z06d
	z03d			z06b; z07b; z07a; z06a	Lb									z06b; z07b; z07a; z06c	z06b; z07b; z07a; z06d
	z03e					Lb				z05a		z05a			
	z03f						Lb				z05b		z05b		
z01b	z03g	z04a						Lb							
	z03h		z04b						Lb						
z01c	z03i					z05a				Lb					
	z03j						z05b				Lb				
z01d	z03k					z05a						Lb			
	z03l						z05b						Lb		
z01e	z03m			z06c; z07a; z06a	z06c; z07a; z07b; z06b									Lb	z06c; z07a; z07b; z06d
	z03n			z06d; z07b; z07a; z06a	z06d; z07b; z06b									z06d; z07b; z07a; z06c	Lb